REMARKS

In the non-final Office Action, the Examiner rejected claims 9-16 and 28 under 35 U.S.C. § 102(e) as anticipated by Cranston et al. (U.S. Patent No. 6,253,269); rejected claims 1, 2, 5-8, 17, 18, 20, 21, 23, and 25-27 under 35 U.S.C. § 103(a) as unpatentable over Jaramillo et al. (U.S. Patent No. 6,598,104) in view of Wang et al. (U.S. Patent Application Publication No. 2004/0098525); rejected claims 3, 19, and 24 under 35 U.S.C. § 103(a) as unpatentable over Jaramillo et al. in view of Wang et al. and Nakamura (U.S. Patent No. 6,622,191); and rejected claims 4 and 22 under 35 U.S.C. § 103(a) as unpatentable over Jaramillo et al. in view of Wang et al. and Melo et al. (U.S. Patent No. 5,553,248).

Applicant respectfully traverses the Examiner's rejection under 35 U.S.C. §§ 102 and 103. Claims 1-28 remain pending.

In paragraph 2 of the Office Action, the Examiner rejected claims 9-16 and 28 under 35 U.S.C. § 102(e) as allegedly anticipated by Cranston et al. Applicant respectfully traverses the rejection.

A proper rejection under 35 U.S.C. § 102 requires that a single reference teach every aspect of the claimed invention either expressly or impliedly. Any feature not directly taught must be inherently present. In other words, the identical invention must be shown in as complete detail as contained in the claim. See M.P.E.P. § 2131. Cranston et al. does not disclose or suggest the combination of features recited in claims 9-16 and 28.

Independent claim 9, for example, recites a method for selecting a bus in a multi-bus system. The method includes generating control signals relating to bus selection in the multi-bus system, determining whether a conflict for bus selection exists based on the control signals,

generating one or more alternate control signals when a conflict is determined to exist, and selecting a bus using the one or more alternate control signals.

Cranston et al. does not disclose or suggest the combination of features recited in claim 9. For example, Cranston et al. does not disclose or suggest generating one or more alternate control signals when a conflict for bus selection is determined to exist. The Examiner alleged that Cranston et al. discloses this feature and cited column 7, lines 17-37, and column 4, lines 1-22, of Cranston et al. for support (Office Action, page 2). Applicant disagrees.

At column 7, lines 17-37, Cranston et al. discloses:

> It should be understood that the arbiter 50 can use a variety of procedures to select between the plurality of communication buses. FIG. 10 shows a general method that can be utilized by the arbiter 50 to select the appropriate communication bus to interface to the application card 20. At Step 100, the arbiter 50 monitors the plurality of communication buses to determine if a communication buses has become active with data from a management card. At Step 102, an active communication bus can be determined in any variety of ways well known to those skilled in the art including monitoring protocols sent on the communication buses.
>
> At Step 104, the active communication bus is allowed access to the application card by connecting or switching the active communication bus to the local bus of the application card. The access to the local card can be provided by a switching function device implemented through an integrated switching matrix, a simple decoder or other solid state integrated circuit. At Step 106, the arbiter prevents the other communication buses from accessing the application card to prevent possible conflicts and contention between the buses.

In this section, Cranston et al. discloses that the arbiter permits access to the application card to an active communication bus and prevents access to other communication buses. Nowhere in this section, or elsewhere, does Cranston et al. disclose generating one or more alternate control signals when a conflict for bus selection is determined to exist, as required by claim 9.

At column 4, lines 1-22, Cranston et al. discloses:

> . . . also possible to combine multiple master devices and multiple slave devices, onto an I^2C-bus to form a multi-master system. In this multi-master system, if more than one

> master device simultaneously attempts to control the line a conflict arises and an arbitration procedure must decide which master device gets priority.
>
> In addition to communication conflicts over a single bus, multiple I^2C-buses accessing the same application card may also potentially conflict. In some systems, several I^2C-buses may exist for redundancy and fault tolerant operation. As previously described, a card chassis holding a number of application cards may include a management card such as Switch Fabric/Management Card 26 to control the operation of the card chassis and application cards within the chassis. To provide for fault tolerant operation, a plurality of management cards may be provided for backup and redundancy. Each of the management cards will have its own communication bus access to each application card. These redundant management communication buses, however, should have mutually exclusive data communication access to the application card to avoid conflicts and contention between multiple devices.

Nowhere in this section, or elsewhere, does Cranston et al. disclose generating one or more alternate control signals when a conflict for bus selection is determined to exist, as required by claim 9.

The Examiner also alleged that Cranston et al. discloses that a priority can be assigned to communication buses and that the priority can be used to allow a communication bus to preempt communication buses of lower priority (Office Action, page 13). The Examiner alleged that the priority assigned to the communication buses "implies" alternate control signals (Office Action, page 2). Applicant disagrees. Assuming that a communication bus priority can be equated to an alternate control signal (a point that Applicant does not concede), Cranston et al. does not disclose or suggest generating a communication bus priority when a conflict for bus selection is determined to exist, as would be required by claim 9. If the Examiner persists with this rejection, Applicant requests that the Examiner specifically identify where Cranston et al. discloses that priorities are generated for the communication buses when a conflict for bus selection is determined to exist.

Because Cranston et al. does not disclose or suggest generating one or more alternate control signals, Cranston et al. cannot disclose or suggest selecting a bus using the one or more alternate control signals, as further recited in claim 9. The Examiner alleged that Cranston et al. discloses this feature and cited column 7, lines 17-56, of Cranston et al. for support (Office Action, page 2). Applicant disagrees.

At column 7, lines 17-56, of which lines 17-37 have been reproduced above, Cranston et al. discloses:

> Because the I^2C-bus is bidirectional, the arbiter also preferably includes knowledge of the I^2C protocol to appropriately switch the bus direction as described above.
>
> Alternatively, the arbiter may select among a plurality of communication buses according to a programmed algorithm or other criteria. A priority can be assigned to communication buses and the priority of the communication bus used to selected the appropriate communication bus to allow access to the application card. A priority can also be utilized to allow a communication bus to preempt communication buses of lower priority. Communication buses may be assigned to classes in which certain classes are allowed simultaneous access to the application card and other classes of communication buses access the card mutually exclusively. The management card may download updated priority scheme to the arbiter over to the I^2C-bus. Using the arbiter, any arbitrary scheme for selecting among a plurality of communication buses may be implemented and tailored and modified according to the needs of the particular device.

In this section, Cranston et al. discloses that buses may be selected based on the priorities assigned to the buses. Nowhere in this section, or elsewhere, does Cranston et al. disclose generating one or more alternate control signals when a conflict for bus selection is determined to exist or selecting a bus using the one or more alternate control signals, as required by claim 9.

For at least these reasons, Applicant submits that claim 9 is not anticipated by Cranston et al. Claims 10-16 depend from claim 9 and are, therefore, not anticipated by Cranston et al. for at least the reasons given with regard to claim 9.

Independent claim 28 recites features similar to features recited in claim 9. Claim 28 is, therefore, not anticipated by Cranston et al. for reasons similar to reasons given with regard to claim 9.

In paragraph 4 of the Office Action, the Examiner rejected claims 1, 2, 5-8, 17, 18, 20, 21, 23, and 25-27 under 35 U.S.C. § 103(a) as allegedly unpatentable over Jaramillo et al. in view of Wang et al. Applicant respectfully traverses the rejection.

Claim 1, for example, recites a system for selecting bus mastership in a multi-master system. The system includes a plurality of master devices and a plurality of slave devices connected to the master devices via a bus. The master devices are configured to generate control signals relating to control of the bus in the multi-master system. Each of the slave devices is configured to receive the control signals from the master devices, determine whether a conflict in the control signals exists, generate one or more alternate control signals for selecting bus mastership when a conflict is determined to exist, and determine which of the master devices obtains control of the bus using the one or more alternate control signals when a conflict is determined to exist.

Neither Jaramillo et al. nor Wang et al., whether taken alone or in any reasonable combination, discloses or suggests the combination of features recited in claim 1. For example, neither Jaramillo et al. nor Wang et al. discloses or suggests a slave device that, for example, is configured to determine whether a conflict exists in control signals received from master devices that relate to control of a bus.

The Examiner alleged that PCI initiators 402-404 correspond to the plurality of master devices recited in claim 1 and PCI target agent 405 corresponds to the plurality of slave devices

recited in claim 1 (Office Action, page 12). The Examiner alleged that Jaramillo et al. discloses a slave device that determines whether a conflict exists based on control signals and cited column 5, lines 52-62, of Jaramillo et al. for support (Office Action, page 5). Applicant disagrees.

At column 5, lines 52-62, Jaramillo et al. discloses:

> FIG. 3 shows a block diagram of a smart retry access process 300 utilized in accordance with one embodiment of the present invention. On the left side of process 300 in step 301, a PCI initiator agent accesses a PCI target agent and attempts a data transmission. The initial access is comprised of the normal stages of a PCI transaction (e.g., arbitration for PCI bus ownership, receiving a grant signal from a PCI arbiter, addressing and informing a PCI target agent of the data to be transferred, etc.). In step 302 the PCI target agent issues a retry in instances where the PCI target agent is busy and cannot complete the data transaction.

In this section, Jaramillo et al. discloses that a PCI initiator agent (master) accesses a PCI target agent (slave) and attempts a data transmission, which involves arbitrating for PCI bus ownership, receiving a grant signal from the PCI arbiter, and informing the PCI target agent of the data to be transferred, and the PCI target agent issues a retry when the PCI target is busy. Nowhere in this section, or elsewhere, does Jaramillo et al. disclose or suggest that a slave device (PCI target agent) determines whether a conflict exists in control signals received from master devices (PCI initiator agents) that relate to control of a bus, as required by claim 1.

In other words, Jaramillo et al. does not disclose or suggest that a PCI target agent determines whether a conflict exists in control signals received from the PCI initiator agents that relate to control of a bus. Instead, PCI target agent issues a retry which denies the PCI initiator agent bus access when PCI target agent is busy with an internal activity, engaging in a transaction that would generate a conflict, or will be slowed in completing a transaction (col. 8, lines 57-61). While Jaramillo et al. discloses that a PCI target agent issues a retry when engaging in a transaction that would generate a conflict, Jaramillo et al. does not disclose or suggest

determining whether a conflict exists in control signals received from master devices that relate to control of a bus, as required by claim 1. Further, Jaramillo et al. discloses that denying the PCI initiator agent bus access permits the PCI bus to be available for use by other PCI initiator agents (col. 5, line 66 - col. 6, line 1). Therefore, any conflict in the PCI target agent has nothing to do with a conflict in control signals from master devices that relate to control of the bus.

Further, Jaramillo et al. clearly discloses that a PCI initiator agent communicates with a PCI target agent only after the PCI initiator agent is granted access to the bus by the PCI arbiter (col. 5, lines 57-59; col. 8, lines 49-52). Jaramillo et al. discloses that the PCI arbiter handles requests for PCI bus ownership (col. 5, lines 57-59; col. 8, lines 49-52).

If the Examiner persists with the rejection of this feature based on Jaramillo et al., Applicant respectfully requests that the Examiner identify the portion of Jaramillo et al. that discloses that a PCI target agent determines whether a conflict exists in control signals from PCI initiator agents relating to control of the bus, as would be required by claim 1. If the Examiner cannot identify any portion of Jaramillo et al. that discloses this feature, the Examiner must withdraw the rejection.

In addition, neither Jaramillo et al. nor Wang et al., whether taken alone or in any reasonable combination, discloses or suggests a slave device that is configured to generate one or more alternate control signals for selecting bus mastership when a conflict in control signals received from the master devices is determined to exist, as further recited in claim 1.

The Examiner alleged that Jaramillo et al. discloses generating one or more alternate control signals for selecting bus mastership when a conflict is determined to exist and cited

column 5, line 52 - column 7, line 18, of Jaramillo et al. for support (Office Action, page 6). Applicant disagrees.

At column 5, line 52 - column 7, line 18, Jaramillo et al. discloses a PCI initiator agent accesses a PCI target agent and attempts a data transmission and the PCI target agent issues a retry in instances where the PCI target agent is busy and cannot complete the data transmission. During, this time, Jaramillo et al. discloses that the PCI arbiter masks requests for the bus from the PCI initiator agent (col. 9, lines 6-15). When the PCI target agent is no longer busy, it signals the PCI arbiter to grant PCI bus access to the PCI initiator agent (col. 6, lines 11-13). Nowhere in this section, or elsewhere, does Jaramillo et al. disclose or suggest that a slave device (PCI target agent) generates one or more alternate control signals for selecting bus mastership when a conflict is determined to exist, as required by claim 1.

The Examiner also alleged that Jaramillo et al. discloses that the PCI target agent includes the ability to access a second signal, which the Examiner alleged was the equivalent of an alternate control signal, indicating the grant status of the PCI bus (Office Action, page 12). Applicant disagrees.

At column 6, lines 58 - column 7, line 2, Jaramillo et al. discloses:

> PCI target agent 405 of the present embodiment includes the ability to access a second signal (hereinafter referred to as the PCI bus grant signal) indicating the grant status of the PCI bus 406. It should appreciated that the PCI bus grant signal is communicated via the grant bus gnt_n (2:0) 502 shown in FIG. 5. The grant bus gnt_n (2:0) 502 is snooped by PCI initiator agents 402, 403 and 404 and, in accordance with the present embodiment, the grant bus gnt_n (2:0) 502 is also snooped by PCI target agent 405. By snooping the grant bus gnt_n (2:0) 502 the PCI target agent 405 can determine which PCI initiator agent is trying to access it.

Even assuming, for the sake of argument, that the PCI bus grant signal (second signal) could be equated to an alternate control signal (a point that Applicant does not concede), Jaramillo et al.

does not disclose or remotely suggest that the PCI bus grant signal is generated by a slave device, as would be required by claim 1. Instead, Jaramillo et al. discloses that the PCI bus grant signal is generated by the PCI arbiter (Fig. 5; col. 6, lines 11-16) and only snooped by the PCI target agent (col. 6, lines 64-67).

If the Examiner persists with the rejection of this feature based on Jaramillo et al., Applicant respectfully requests that the Examiner identify the portion of Jaramillo et al. that discloses that a PCI target agent generates one or more alternate control signals for selecting bus mastership when a conflict in control signals received from the PCI initiator agents is determined to exist, as would be required by claim 1. If the Examiner cannot identify any portion of Jaramillo et al. that discloses this feature, the Examiner must withdraw the rejection.

In addition, neither Jaramillo et al. nor Wang et al. discloses or suggests a slave device that is configured to determine which of the master devices obtains control of the bus using one or more alternate control signals generated when a conflict is determined to exist, as required by claim 1. The Examiner admitted that Jaramillo et al. does not disclose this feature and relied on Wang et al. for allegedly disclosing the feature and cited paragraph 0027 of Wang et al. for support (Office Action, page 6). Applicant disagrees.

At paragraph 0027, Wang et al. discloses:

> The arbiter 310 arbitrates the access requests from the N master processors via the N master buses. The arbiter 310 generates arbitration signals as result of the arbitration. The arbitration signals indicate which master processor is given access to the slave device if there is access conflict. The corresponding master processors are informed of the arbitration so that it can proceed with the access if the access is granted, or attempt to access again if the access is denied.

The arbiter that Wang et al. refers to in this section is a part of the system bus controller illustrated in Figure 1. Nowhere in this section, or elsewhere, does Wang et al. disclose or

remotely suggest that a slave device is configured to determine which of the master devices obtains control of the bus using one or more alternate control signals generated by the slave device when a conflict exists in control signals relating to control of the bus from the master devices, as required by claim 1.

For at least these reasons, Applicant submits that claim 1 is patentable over Jaramillo et al. and Wang et al., whether taken alone or in any reasonable combination. Claims 2 and 5-7 depend from claim 1 and are, therefore, patentable over Jaramillo et al. and Wang et al. for at least the reasons given with regard to claim 1. Claims 2 and 5-7 are also patentable over Jaramillo et al. and Wang et al. for reasons of their own.

For example, claim 2 recites bus selection logic that is configured to determine whether the control signals indicate that two or more of the master devices concurrently assert control of the bus and generate a conflict indication signal when two or more of the master devices concurrently assert control of the bus, and conflict resolution logic that is configured to generate the one or more alternate control signals in response to the conflict indication signal. Neither Jaramillo et al. nor Wang et al., whether taken alone or in any reasonable combination, discloses or suggests this combination of features. For example, neither Jaramillo et al. nor Wang et al. discloses or suggests bus selection logic that is configured to determine whether the control signals indicate that two or more of the master devices concurrently assert control of the bus and generate a conflict indication signal when two or more of the master devices concurrently assert control of the bus.

The Examiner alleged that Jaramillo et al. discloses bus selection logic and cited column 5, line 52 - column 6, line 40, of Jaramillo et al. for support (Office Action, page 6). Applicant disagrees.

At column 5, line 52 - column 6, line 40, Jaramillo et al. discloses that a PCI initiator agent accesses a PCI target agent and attempts a data transmission and the PCI target agent issues a retry in instances where the PCI target agent is busy and cannot complete the data transmission. When the PCI target agent is no longer busy, it signals the PCI arbiter to grant PCI bus access to the PCI initiator agent. Nowhere in this section, or elsewhere, does Jaramillo et al. disclose or suggest, for example, a slave device that determines whether the control signals indicate that two or more of the master devices concurrently assert control of the bus, as recited in claim 2.

Instead, Jaramillo et al. discloses that a PCI target agent issues a retry when the PCI target agent is busy and cannot complete a transaction (col. 5, lines 60-62). Jaramillo et al. is concerned with PCI target agent availability and not bus conflicts as evident by the fact that Jaramillo et al. discloses that a PCI initiator agent that has received a retry signal from one PCI target agent can access the bus for purposes of communicating with other PCI target agents (col. 6, lines 33-40). Further, Jaramillo et al. clearly discloses that a PCI initiator agent communicates with a PCI target agent only after the PCI initiator agent is granted access to the bus by the PCI arbiter (col. 5, lines 57-59; col. 8, lines 49-52). Jaramillo et al. discloses that the PCI arbiter handles requests for PCI bus ownership (col. 5, lines 57-59; col. 8, lines 49-52).

The Examiner also alleged that Jaramillo et al. discloses that a PCI target agent includes the ability to access a second signal (which the Examiner alleged is equivalent to an alternate control signal) indicating the grant status of the PCI bus (Office Action, page 13). Jaramillo et

al. discloses that this "second" signal (i.e., PCI bus grant signal) indicates which PCI initiator agent is granted access to the bus. Nowhere does Jaramillo et al. disclose or remotely suggest that the PCI target agent (slave device) uses the PCI bus grant signal to determine whether control signals indicate that two or more of the PCI initiator agents (master devices) concurrently assert control of the bus, but instead indicates to the PCI target agent which of the PCI initiator agents is currently granted bus access.

For at least these additional reasons, Applicant submits that claim 2 is patentable over Jaramillo et al. and Wang et al., whether taken alone or in any reasonable combination.

Claim 6 recites that the control signals include a present signal that indicates whether a corresponding one of the master devices is operating and a master signal that indicates whether a corresponding one of the master devices asserts control of the bus. Neither Jaramillo et al. nor Wang et al., whether taken alone or in any reasonable combination, discloses or suggests this combination of features. For example, neither Jaramillo et al. nor Wang et al. discloses or suggests a present signal that indicates whether a corresponding one of the master devices is operating.

The Examiner alleged that Jaramillo et al. discloses a present signal and cited column 5, line 52 - column 6, line 40, of Jaramillo et al. for support (Office Action, page 8). Applicant disagrees.

Contrary to the Examiner's allegation, nowhere in column 5, line 52 - column 6, line 40, or elsewhere, does Jaramillo et al. disclose or suggest anything resembling a present signal that indicates whether a corresponding one of the master devices is operating, as recited in claim 6. In Applicant's prior response, Applicant requested that the Examiner specifically identify which

signal in Jaramillo et al. allegedly corresponds to the present signal recited in claim 6. The Examiner did not identify any signal, but merely repeated the same rejection (Office Action, page 8).

If the Examiner again persists with this rejection of claim 6, Applicant requests that the Examiner specifically identify which signal in Jaramillo et al. allegedly corresponds to the present signal recited in claim 6. If the Examiner cannot identify any allegedly equivalent signal in Jaramillo et al., the Examiner must withdraw the rejection.

For at least these additional reasons, Applicant submits that claim 6 is patentable over Jaramillo et al. and Wang et al., whether taken alone or in any reasonable combination.

Independent claim 8 recites a system for selecting a master in a multi-master system. The system includes means for outputting first and second control signals relating to mastership in the multi-master system from each of a plurality of masters in the multi-master system, means for determining whether a conflict for mastership exists based on the first and second control signals, means for generating a switch signal and a select signal when a conflict is determined to exist, and means for selecting one of the masters using the switch signal and the select signal.

Neither Jaramillo et al. nor Wang et al., whether taken alone or in any reasonable combination, discloses or suggests the combination of features recited in claim 8. For example, neither Jaramillo et al. nor Wang et al. discloses or suggests means for outputting first and second control signals relating to mastership in the multi-master system from each of a plurality of masters in the multi-master system. The Examiner alleged that Jaramillo et al. discloses means for outputting first and second control signals relating to mastership and cited column 5, lines 52-62, of Jaramillo et al. for support (Office Action, page 8). Applicant disagrees.

Column 5, lines 52-62, of Jaramillo et al. has been reproduced above. Nowhere in this section, or elsewhere, does Jaramillo et al. disclose or suggest means for outputting first and second control signals relating to mastership in the multi-master system from each of a plurality of masters in the multi-master system, as required by claim 8.

If the Examiner persists with the rejection of this feature based on Jaramillo et al., Applicant requests that the Examiner specifically identify which signals in Jaramillo et al. allegedly correspond to the first and second control signals recited in claim 8. If the Examiner cannot identify signals that correspond to the first and second control signals, then the Examiner must withdraw the rejection.

In addition, neither Jaramillo et al. nor Wang et al. discloses or suggests means for generating a switch signal and a select signal when a conflict for mastership is determined to exist, as further recited in claim 8. The Examiner alleged that Jaramillo et al. discloses this feature and cited column 5, line 52 - column 6, line 40, of Jaramillo et al. for support (Office Action, page 9). Applicant disagrees.

At column 5, line 52 - column 6, line 40, Jaramillo et al. discloses that a PCI initiator agent attempts to perform a data transaction with a PCI target agent and the PCI target agent issues a retry when the PCI target agent is busy and cannot complete the data transaction. Nowhere in this section, or elsewhere, does Jaramillo et al. disclose or suggest means for generating a switch signal and a select signal when a conflict for mastership is determined to exist, as required by claim 8.

If the Examiner persists with the rejection of this feature based on Jaramillo et al., Applicant requests that the Examiner specifically identify which signals in Jaramillo et al.

allegedly correspond to the switch and select signals recited in claim 8. If the Examiner cannot identify signals that correspond to the switch and select signals, then the Examiner must withdraw the rejection.

For at least these reasons and reasons similar to reasons given above with regard to claim 1, Applicant submits that claim 8 is patentable over Jaramillo et al. and Wang et al., whether taken alone or in any reasonable combination.

Independent claim 17 recites features similar to features recited in claim 8. Claim 17 is, therefore, patentable over Jaramillo et al. and Wang et al., whether taken alone or in any reasonable combination, for reasons similar to reasons given with regard to claim 8.

Independent claim 18 recites features similar to features recited in claim 2. Claim 18 is, therefore, patentable over Jaramillo et al. and Wang et al., whether taken alone or in any reasonable combination, for reasons similar to reasons given with regard to claim 2. Claims 20 and 21 depend from claim 18 and are, therefore, patentable over Jaramillo et al. and Wang et al. for at least the reasons given with regard to claim 18. Claim 20 also recites features similar to features recited in claim 6. Claim 20 is, therefore, also patentable over Jaramillo et al. and Wang et al. for reasons similar to reasons given with regard to claim 6.

Independent claim 23 recites features similar to features recited in claim 2. Claim 23 is, therefore, patentable over Jaramillo et al. and Wang et al., whether taken alone or in any reasonable combination, for reasons similar to reasons given with regard to claim 2. Claims 25 and 26 depend from claim 23 and are, therefore, patentable over Jaramillo et al. and Wang et al. for at least the reasons given with regard to claim 23. Claim 25 also recites features similar to

features recited in claim 6. Claim 25 is, therefore, also patentable over Jaramillo et al. and Wang et al. for reasons similar to reasons given with regard to claim 6.

Independent claim 27 recites a multi-master system that includes a plurality of master devices, conflict resolution logic, and a plurality of slave devices. The master devices are configured to generate control signals relating to bus mastership. The conflict resolution logic is configured to receive the control signals from the master devices, determine whether the control signals indicate that two or more of the master devices concurrently assert bus mastership, and generate a switch signal and a select signal when it is determined that two or more of the master devices concurrently assert bus mastership. The slave devices are configured to select bus mastership using the switch signal and the select signal when the control signals indicate that two or more of the master devices concurrently assert bus mastership.

Initially, Applicant submits that the Examiner's rejection of claim 27 is deficient for several reasons. For example, the Examiner rejected claim 27 based on a combination of Jaramillo et al. and Wang et al. In the rejection of the features of claim 27, however, the Examiner relied only on the Jaramillo et al. reference for allegedly disclosing every feature of claim 27. The Examiner cited no portion of Wang et al. and provided no motivation for combining the alleged features of Jaramillo et al. and Wang et al. Therefore, the Examiner's rejection of claim 27 based on a combination of Jaramillo et al. and Wang et al. is improper.

Nevertheless, neither Jaramillo et al. nor Wang et al., whether taken alone or in any reasonable combination, discloses or suggests the combination of features recited in claim 27. For example, neither Jaramillo et al. nor Wang et al. discloses or suggests conflict resolution logic that is configured to, for example, generate a switch signal and a select signal when it is

determined that two or more of the master devices concurrently assert bus mastership. The Examiner alleged that Jaramillo et al. discloses these features and cited column 6, line 18 - column 7, line 18, of Jaramillo et al. for support (Office Action, pages 9-10). Applicant disagrees.

At column 6, line 18 - column 7, line 18, Jaramillo et al. discloses that when a PCI initiator agent attempts to access a PCI target agent, the PCI target agent issues a bus denial signal to the PCI arbiter so that the PCI arbiter will deny the PCI initiator agent bus access. Nowhere in this section, or elsewhere, does Jaramillo et al. disclose conflict resolution logic that generates a switch signal and a select signal when it is determined that two or more master devices concurrently assert bus mastership.

If the Examiner persists with the rejection of this feature based on Jaramillo et al., Applicant requests that the Examiner specifically identify which signals in Jaramillo et al. allegedly correspond to the switch and select signals recited in claim 27. If the Examiner cannot identify signals that correspond to the switch and select signals, then the Examiner must withdraw the rejection.

In addition, neither Jaramillo et al. nor Wang et al. discloses or suggests a plurality of slave devices that are configured to select bus mastership using the switch signal and the select signal when the control signals indicate that two or more of the master devices concurrently assert bus mastership, as further recited in claim 27. The Examiner alleged that Jaramillo et al. discloses these features and cited column 6, lines 18-67, of Jaramillo et al. for support (Office Action, page 10). Applicant disagrees. Because Jaramillo et al. does not disclose a switch signal and a select signal, Jaramillo et al. cannot disclose or suggest a slave device that is configured to

select bus mastership using the switch signal and the select signal when the control signals indicate that two or more of the master devices concurrently assert bus mastership, as recited in claim 27.

For at least these reasons, Applicant submits that claim 27 is patentable over Jaramillo et al. and Wang et al., whether taken alone or in any reasonable combination.

In paragraph 5 of the Office Action, the Examiner rejected claims 3, 19, and 24 under 35 U.S.C. § 103(a) as allegedly unpatentable over Jaramillo et al. in view of Wang et al. and Nakamura.

Claims 3, 19, and 24 depend from claims 1, 18, and 23, respectively. While not acquiescing in the Examiner's rejection, Applicant submits that the disclosure of Nakamura does not cure the deficiencies in the disclosures of Jaramillo et al. and Wang et al. identified above with regard to claims 1, 18, and 23. Therefore, claims 3, 19, and 24 are patentable over Jaramillo et al., Wang et al., and Nakamura, whether taken alone or in any reasonable combination, for at least the reasons given with regard to claims 1, 18, and 23.

In paragraph 6 of the Office Action, the Examiner rejected claims 4 and 22 under 35 U.S.C. § 103(a) as allegedly unpatentable over Jaramillo et al. in view of Wang et al. and Melo et al.

Claims 4 and 22 depend from claims 1 and 18, respectively. While not acquiescing in the Examiner's rejection, Applicant submits that the disclosure of Melo et al. does not cure the deficiencies in the disclosures of Jaramillo et al. and Wang et al. identified above with regard to claims 1 and 18. Therefore, claims 4 and 22 are patentable over Jaramillo et al., Wang et al., and

Melo et al., whether taken alone or in any reasonable combination, for at least the reasons given with regard to claims 1 and 18.

In view of the foregoing remarks, Applicant respectfully requests the Examiner's reconsideration of the application and the timely allowance of pending claims 1-28.

If the Examiner does not believe that all pending claims are now in condition for allowance, the Examiner is urged to contact the undersigned to expedite prosecution of this application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1070 and please credit any excess fees to such deposit account.

Respectfully submitted,

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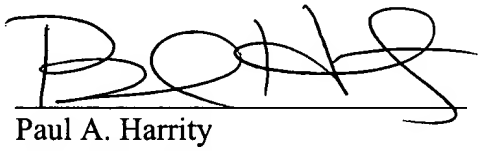

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